AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A pixel sensor ~~for providing image sensing under radiation or space environment,~~ comprising:

an n-type photosensitive element for converting an optical image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a readout circuit ~~operating to convert optical image signals to electronic signals, where said readout circuit includes p-type transistors and an n-type photosensitive element~~ coupled to said source follower transistor and comprising a p-type transistor; and

a first reset circuit configured to provide a reset signal ~~level for a pixel output~~ at said gate of said source follower transistor, where said first reset circuit includes at least one p-type transistor~~,~~

~~where said readout circuit and said first reset circuit having said p-type transistors, and said n-type photosensitive element, provide radiation hardness without any radiation protective enclosure~~.

2. (Original) The pixel sensor of claim 1, wherein said p-type transistors are MOSFET p-type transistors.

3. (Original) The pixel sensor of claim 1, wherein said n-type photosensitive element is an n-type photodiode.

4. (Original) The pixel sensor of claim 3, wherein said n-type photodiode is formed in a square layout design.

5. (Original) The pixel sensor of claim 3, wherein said n-type photodiode is formed in a circular layout design.

6. (Currently Amended) The pixel sensor of claim 1, further comprising:

a p-type substrate ~~on~~ in which said n-type photosensitive element is formed.

7. (Currently Amended) The pixel sensor of claim 6, further comprising:

a pair of p+ type guard rings formed ~~on~~ in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings ~~connected~~ adapted for connection to a ground voltage, and operating to ~~substantially~~ reduce a leakage current from said n-type photosensitive element.

8. (Currently Amended) The pixel sensor of claim 6, further comprising:

an n-type well ~~provided adjacent to~~ formed in said p-type substrate, said n-type well ~~connected~~ adapted for connection to a supply voltage, and operating to prevent ~~crosstalk between pixels~~ charges from escaping the pixel sensor.

9. (Original) The pixel sensor of claim 1, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

10. (Currently Amended) ~~A radiation-hard CMOS~~ An image sensing device, comprising:

a p-type substrate;

an n-type photodiode formed ~~on~~ in said p-type substrate, where said n-type photodiode operates to convert an optical ~~signal~~ image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset circuit configured to provide a reset ~~value~~ signal for said electrical signal, said first reset circuit including a p-type MOSFET transistor; and

a readout circuit operating to buffer said electrical signal, said readout circuit including a p-type MOSFET transistor.

11. (Currently Amended) The device of claim 10, further comprising:

a pair of p+ type guard rings formed ~~on~~ in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photodiode, said pair of guard rings ~~connected~~ adapted for connection to a ground voltage, and operating to ~~substantially~~ reduce a leakage current from said n-type photodiode.

12. (Currently Amended) The device of claim 11, further comprising:

an n-type well provided adjacent to ~~said p-type substrate~~ one of said pair of p+ type guard rings, said n-type well ~~connected~~ adapted for connection to a supply voltage, and operating to prevent crosstalk between pixels in the ~~CMOS~~ image sensing device.

13. (Original) The device of claim 10, further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

14. (Currently Amended) A CMOS image sensor system, comprising:

an array of active pixel sensors, each pixel sensor of said array including:

~~a pixel readout circuit~~ an n-type photosensitive element operating to convert an optical image ~~signals~~ to ~~electronic signals~~ an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a pixel readout circuit, where said pixel readout circuit includes at least one p-type ~~transistors~~ transistor coupled to receive an output of said source follower transistor; ~~and an n-type photosensitive element,~~ and

a first reset circuit configured to provide a reset level for a pixel output signal, where said first reset circuit includes at least one p-type ~~transistors,~~ transistor;

~~where said pixel readout circuit and said first reset circuit having said p-type transistors and said n-type photosensitive element provide radiation hardness without any radiation protective enclosure;~~

a control circuit configured to provide timing and control signals to enable read out of data stored in said array of active pixel sensors; and

a column readout circuit operating to receive and process said data stored in said array of active pixel sensors.

15. (Currently Amended) The CMOS image sensor of claim 14, further comprising:

a p-type substrate ~~on~~ in which said ~~n-type photosensitive element~~ array of pixel sensors is formed.

16. (Currently Amended) The CMOS image sensor of claim 15, each pixel sensor further comprising:

a pair of p+ type guard rings formed ~~on~~ in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings ~~connected~~ adapted for connection to a ground voltage, and operating to ~~substantially~~ reduce a leakage current from said n-type photosensitive element.

17. (Currently Amended) The CMOS image sensor of claim 15, each pixel sensor further comprising:

an n-type well provided adjacent to ~~said p-type substrate~~ at least one of said pair of p+ type guard rings, said n-type well ~~connected~~ adapted for connection to a supply voltage, and operating to prevent crosstalk between pixels.

18. (Currently Amended) The CMOS image sensor of claim 14, each pixel sensor further comprising:

a second reset circuit having a p-type MOSFET transistor coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

19. (New) The pixel sensor of claim 1, wherein the p-type transistor of the readout circuit comprises a row select transistor for selectively reading out said pixel output signal.

20. (New) The pixel sensor of claim 19, wherein said row select transistor is coupled to receive an output of said source follower transistor.

21. (New) The device of claim 10, wherein the device is a CMOS image sensing device and said p-type transistors provide radiation hardness without any radiation protective enclosure.

22. (New) The device of claim 10, wherein said source follower transistor is a p-type MOSFET transistor.

23. (New) The device of claim 10, wherein the readout circuit comprises a row select transistor for selectively outputting said pixel output signal.

24. (New) The device of claim 23, wherein said row select transistor is coupled to receive an output of said source follower transistor.

25. (New) The CMOS image sensor of claim 14, wherein said readout circuit includes a row select transistor for selectively connecting the pixel sensor to a column line of the array.

26. (New) The CMOS image sensor of claim 25, wherein said row select transistor is coupled to receive said output of said source follower transistor.

27. (New) The CMOS image sensor of claim 14, wherein said p-type transistors provide radiation hardness to the array of active pixel sensors.

28. (New) An array of pixel sensors comprising:

a plurality of pixels formed in a p-type substrate, at least one of said pixels comprising:

an n-type photodiode formed in said substrate and for generating an electrical signal in response to an applied optical image;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset circuit coupled to said gate and responsive to a first reset signal for providing a global reset value as said pixel output signal;

a second reset circuit coupled to an input of said first reset circuit and responsive to a second reset signal for operating said first reset circuit to allow a pixel-by-pixel reset;

a p-type row select transistor for selectively connecting the pixel to an associated column line of the array for readout of the pixel output signal; and

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings located on either side of said n-type photodiode.

29. (New) The array of pixel sensors of claim 28, said at least one pixel further comprising an n-type well located adjacent at least one of said pair of p+ type guard rings in said p-type substrate.

30. (New) The array of pixel sensors of claim 28, wherein said p-type transistors provide said at least one pixel with radiation hardness, without a radiation protective enclosure.